REMARKS

Reconsideration of the application is respectfully requested.

The objection to the Drawing is noted. However, the Examiner is respectfully asked to review Figures 1 and 2 and note that blocks labeled 1-3 are descriptively labeled just below and to the right of the block diagram of Figure 1, and, block 21 in Figure 2 is the label "Degaussing" which is understood in the art.

The title has been amended to read "Mains Frequency Synchronous Burst Mode Power Supply".

Independent claims 1, 12 and 20 have been amended to recite "a momentary amplitude of". This additional claim language makes it clear that the gate circuit does not initiate a burst of output pulses, in the case of claims 1 and 20, or enable operation of the self-oscillating power converter, in the case of claim 12, until a momentary amplitude of the AC mains supply is within or through a predetermined range.

Claims 1-19 have also been amended to delete reference characters and numbers, as is customary in U.S. practice.

A copy of filed claims 1-20 with manuscript interlineations is included to show how the claims have been amended.

Claims 1-25 have been rejected under 35 USC 102(b) as being anticipated by the patent 5,369,561 to McCullough. New claims 1, 12 and 20 have been amended to claim that the gate circuit initiating the burst of output pulses or enablement of the self-oscillating power converter, in the case of claim 12 when a momentary amplitude of the AC mains supply is within a predetermined range.

In contrast, McCullough discloses that if an RMS voltage drops below a predetermined level or state, the AC inverter starts running. Unlike the claimed invention where there is no bursting of output pulses or power conversion operation is not enabled when the AC mains supply amplitude is below a certain level, McCullough makes voltage when its RMS drops below a certain level. The claimed invention is directed to generating DC power more efficiently by ceasing conversion when amplitude of the mains is below a desired range, whereas McCullough is directed to generating AC power supply during all of an AC sinusoidal cycle.

As noted in Figure 1 of McCullough, the switch K1 is merely toggled to pass a line input voltage, from the utility company supply, to an output load. The variable frequency inversion for preventing saturation of magnetic components, taught by McCullough, neither discloses nor suggests the claimed invention of bursting output pulses derived from an AC mains supply when a momentary amplitude of that AC mains supply is within a predetermined range.

The prior art made of record has been considered by the Applicant and is deemed to neither disclose nor suggest, alone or in combination, with McCullough, the claimed invention.

Should the Examiner feel that anything further is necessary to place this application in condition for allowance, he is respectfully requested to contact Applicant's attorney at the telephone number listed below.

Respectfully submitted,

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CLAIMS:

1. A synchronous burst mode power supply comprising:

a power converter ~~(2)~~ for transforming an AC mains from a relatively low frequency to a higher frequency; and

a gate circuit ~~(1)~~ responsive to said AC mains supply for enabling said power converter ~~(2)~~ to initiate a burst of output pulses at said higher frequency each time said AC mains supply occurs within a predetermined range. a momentary amplitude of

2. The power supply according to claim 1, further comprising means ~~(3)~~ for regulating a transformed output ~~(V3)~~ from said converter circuit ~~(2)~~ to a standby voltage ~~(Vout)~~, said means ~~(3)~~ being coupled back to said gate circuit ~~(1)~~ for controlling operation of said power converter circuit ~~(2)~~ in response to load changes to said power supply.

3. The power supply according to claim 1, wherein said power converter ~~(2)~~ comprises a self-oscillating circuit ~~(Block 2)~~ and said gate circuit ~~(Block 1)~~ enables operation of said self-oscillating circuit only during two periods of each cycle of said supply ~~(V1)~~ from said AC mains when said supply ~~(V1)~~ has a single voltage polarity.

4. The power supply according to claim 1, wherein said gate circuit comprises a threshold detector circuit ~~(22)~~ for generating voltage pulses ~~(V2)~~ when detecting portions of positive waveforms ~~(V1)~~ of said mains voltage within said predetermined range.

5. The power supply according to claim 4, wherein said threshold detector ~~(22)~~ comprises a transistor ~~(Q1)~~ biased at its base terminal by a first voltage division ~~(R1, R2)~~ of said positive waveforms ~~(V1)~~ to pass said voltage pulses ~~(V2)~~ from a second voltage division of said positive waveforms ~~(V1)~~.

6. The power supply circuit of Claim 5, wherein said first voltage division comprises a resistor pair ~~(R1, R3)~~ divider coupled to a base terminal B of said transistor ~~(Q1)~~, and said second voltage division comprises a resistor pair ~~(R4, R5)~~ coupled to said positive waveforms ~~(V1)~~ and an emitter terminal of said transistor ~~(Q1)~~.

7. The power supply circuit of Claim 4, wherein said power converter circuit ~~(2)~~ comprises a free running oscillator circuit ~~(23)~~ for converting said voltage pulses ~~(V2)~~ from said gate circuit ~~(1)~~ at a first frequency to current pulses ~~(IT1)~~ at a second frequency greater than said first frequency.

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8. The power supply circuit of Claim 7, wherein said free running oscillator circuit (23) comprises a transistor (Q2) biased at its base terminal B by said voltage pulses (V2) that are rectified by a first diode and then charge a first capacitor (C3) for enabling said second transistor (Q2) to conduct said current pulses (ITr), said current pulses (ITr) being derived from said positive waveforms (V1) ripple attenuated by a second capacitor (C4) coupled to an emitter terminal of said second transistor (Q2), said positive waveforms (V1) energizing a primary winding (n1) of a transformer (TR1) to develop in a flyback manner a secondary winding voltage (VTR1) across a secondary winding (n2) of said transformer (TR1).

9. The power supply circuit of Claim 7, further comprising a voltage regulating circuit (24) coupled to a secondary winding (n2) of a transformer (TR1) having a primary winding (n1) coupled to said free running oscillator circuit (2), said secondary winding (n2) developing a secondary voltage (VTR1) from said current pulses (ITr) conducted through a primary winding (n1) of said transformer (TR1).

10. The power supply circuit of Claim 9, wherein said voltage regulating circuit (24) comprises an integrated voltage regulator (IC1) coupled to a diode D6 and a first capacitor (C3) arrangement for rectifying and filtering said current pulses (ITr) from said secondary winding (n2) to provide a secondary voltage (V3) stabilized by said integrated voltage regulator (IC1), said secondary voltage being filtered by a second capacitor (C6) to provide a standby voltage (Vout).

11. The power supply circuit of Claim 7, further comprising a voltage regulating circuit (244) coupled to a secondary winding (n2) of a transformer (TR1) having a primary winding (n1) through which said current pulses (ITr) controllably conduct to develop a secondary winding voltage (VTR1) that is coupled back to and adjust on-time operation of said threshold detector circuit (222).

12. A synchronous burst mode standby power supply comprising:

a self-oscillating power converter for receiving an AC mains supply;

a transformer primary winding coupled to said power converter and receiving pulses therefrom for generating a supply of power at a secondary winding of said transformer; and

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a gate circuit coupled to said AC mains supply and said power converter, wherein said gate circuit enables operation of said self-oscillating power converter while said AC mains supply cycles through a predetermined range.

13. The power supply circuit of claim 12, wherein said gate circuit comprises a threshold detector (~~22~~) for generating voltage pulses (~~V2~~) when detecting positive waveforms (~~V1~~) of said mains voltage below a threshold.

14. The power supply circuit of Claim 13, wherein said threshold detector (~~22~~) comprises a transistor (~~Q1~~) biased at its base terminal by a first voltage division (~~R1, R2~~) of said positive waveforms (~~V1~~) to pass said voltage pulses (~~V2~~) from a second voltage division and filtering of said positive waveforms (~~V1~~).

15. The power supply circuit of Claim 14, wherein said first voltage division comprises a first resistor pair (~~R1, R3~~) divider coupled to a base terminal B of said transistor (~~Q1~~), and said second voltage division comprises a second resistor pair (~~R4, R5~~) coupled between said positive waveforms (~~V1~~) and an emitter terminal of said transistor (~~Q1~~).

16. The power supply circuit of Claim 2, wherein said self-oscillating power converter circuit converts said voltage pulses (~~V2~~) at a first frequency to current pulses (~~ITr~~) at a second frequency greater than said first frequency.

17. The power supply circuit of Claim 16, further comprising a voltage regulating circuit (~~244~~) coupled to a secondary winding (~~n2~~) of a transformer (~~TR1~~) having a primary winding (~~n1~~) through which said current pulses (~~ITr~~) controllably conduct to develop a secondary winding voltage (~~VTR1~~) that is coupled back to said threshold detector (~~222~~) for influencing on-time operation of said self-oscillating power converter.

18. The power supply circuit of Claim 17, wherein said voltage regulating circuit (~~244~~) comprises an integrated voltage regulator (~~IC1~~), coupled to a diode D6 and capacitor (~~C5~~) arrangement, for receiving said secondary winding voltage (~~VTR1~~) and providing a voltage input (~~V3~~) for said integrated voltage regulator (~~IC1~~), and an opto-coupler (~~IC2~~) coupled to said integrated voltage regulator (~~IC1~~) for conducting current derived from said secondary winding voltage (~~VTR1~~) back to said threshold detector (~~222~~) when said voltage input (~~V3~~) is above a reference voltage.

19. The power supply circuit of claim 18, wherein said reference voltage is developed across a resistor (R8) and zener diode (D7) arrangement coupled between the voltage input (V3) and said opto-coupler (IC2).

20. A method for providing synchronous burst mode power comprising the steps of:

receiving an AC mains supply at a relatively low frequency; a momentary amplitude of

detecting when said AC mains supply occurs within a predetermined range; and

initiating a burst of output pulses at a higher frequency than said relatively low frequency responsive to said detecting step

21. The method according to claim 20, further comprising the step of terminating further initiation of said burst of output pulses responsive to said detecting.

22. The method according to claim 20, wherein said detecting step comprises when said AC mains occurs below a first threshold and above a second threshold.

23. The method according to claim 20, further comprising the step of regulating said output pulses to a standby voltage output.

24. The method according to claim 20, further comprising the step of controlling timing of said initiating by a voltage derived from said output pulses.

25. The method according to claim 21, further comprising the step of controlling timing of said initiating and terminating by a voltage derived from said output pulses.

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